

WHAT IS CLAIMED IS:

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1. ~~A method for pulse width modulation comprising the steps of:
providing a pulse width modulator having n bits of resolution and a nominal
time period P_n ;
supplying an additional timer to generate K associated states and having a
timer period P_T ;
associating a modulator output value with each one of said K states; and
establishing a pulse width modulation update interval of $K \cdot P_T$.~~
 2. The method of claim 1 wherein P_T is an integer multiple of P_n .
 3. The method of claim 1 wherein said pulse width modulator includes an
overflow bit.
 4. ~~The method of claim 1 wherein $P_T = P_n$.~~
 5. ~~A method for improving the resolution of an n bit pulse width
modulator having a nominal time period of P_n , the method comprising the steps of:
supplying an additional timer having K associated states and a timer period of
 P_T ;
associating a modulator output value with each one of said K states; and
outputting a pulse according to said modulator output value during each time
period P_n occurring within said timer period P_T during each one of said K timer states,
whereby the resolution of said n bit pulse width modulator substantially equals $n = \log_2(K)$.~~
 6. The method of claim 5 wherein P_T is an integer multiple of P_n .
 7. The method of claim 5 wherein said pulse width modulator includes an
overflow bit.
 8. The method of claim 5 wherein $P_T = P_n$.
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1 9. The method of claim 5 where P_T is other than an integer multiple of
2 P_n and $P_T \gg P_n$.

1 10. The method of claim 9 wherein said pulse width modulator includes an
overflow bit.

3 11. A computer program product for pulse width modulation comprising:
4 a computer readable storage medium having computer readable
5 program code means embedded in said medium, said computer readable program code means
6 having:

7 a first computer instruction means for associating K timer states with a
8 timer having a period P_T ; and

9 a second computer instruction means for reading a commanded pulse
10 width modulation duty cycle;

11 a third computer instruction means for assigning an n bit modulator
12 output value with each one of said K states according to said duty cycle.

1 12. The computer program product of claim 11 wherein said third
2 computer instruction means updates said n bit modulator output value assigned to each state
3 at time intervals of $K \cdot P_T$.

1 13. A method for controlling the brightness of a display using pulse width
2 modulation comprising the steps of:

3 receiving a commanded brightness level;

4 using an n bit pulse width modulator to assert a plurality of pulses in
5 accordance with an output of said n bit pulse modulator wherein said modulator has a period
6 P_n ;

7 assigning a modulator output value to each one of K states of a K state timer
8 wherein said timer has a period P_T ;

9 outputting said plurality of pulses according to said modulator output value
10 during each P_n period occurring within timer period P_T ; and

11 supplying power to the display in accordance with said plurality of pulses.

1 14. An apparatus for pulse width modulation comprising:
2 an n bit pulse width modulator having a nominal modulator period P_n ;
3 a timer to generate K timer states and having a timer period P_T ;
4 a computing device for assigning a modulator output value to each of said K
5 states; and
6 whereby said modulator outputs a plurality of pulses according to said
7 modulator output value during each P_n period occurring within timer period P_T and whereby
8 said pulse width modulator has a resolution of $n + \log_2 K$.

1 15. The apparatus of claim 14 wherein said timer is included within said
2 computing device.

1 16. The apparatus of claims 14 where P_T is an integer multiple of P_n .

1 17. The apparatus of claim 14 wherein P_T is other than an integer multiple
2 of P_n and $P_T \gg P_n$.

1 18. The apparatus of claim 14 wherein said modulator further comprises
2 overflow bit.

1 19. An apparatus improving the resolution of an n bit pulse width
2 modulator having a P_n period, the apparatus comprising:
3 a timer to generate K timer states and having a timer period P_T ;
4 a computing device for assigning a modulator output value to each of said K
5 states; and
6 whereby said modulator outputs a plurality of pulses according to a modulator
7 output value during each P_n period occurring within timer period P_T and whereby the pulse
8 width modulator has a resolution of $n + \log_2 K$.

1 20. An LED backlit display comprising:
2 an array of LEDs;
3 an n bit pulse width modulator having a period of P_n ;

a computing device for assigning a modulator output value to each of said K states;

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